

# *MESI MODEL*

- ❑ CACHE CONSISTENCY MODEL FOR MULTIPROCESSING ENVIRONMENT, WITH FOUR STATES - MODIFIED, EXCLUSIVE, SHARED, AND INVALID
- ❑ EVERY CACHE LINE IS ASSIGNED ONE OF THESE STATES INDICATORS TO IDENTIFY THE STATUS OF THE INFORMATION STORED IN CACHE
- ❑ TRANSITIONS FROM ONE STATE TO ANOTHER MAY BE TRIGGERED BY A LOCAL PROCESSOR READ OR WRITE OR A BUS SNOOP WHEN ANOTHER BUS MASTER INITIATES BUS ACTIVITIES
- ❑ DURING RESET, THE MESI STATES BITS FOR L1 AND L2 CACHE ARE SET TO INVALID STATE (I)

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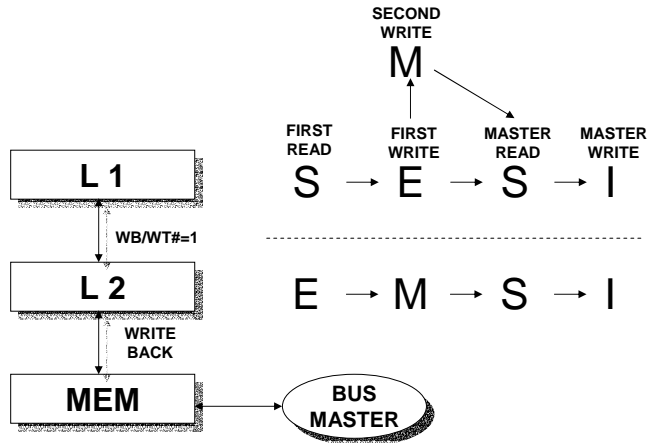
STUDY THE MESI PROTOCOL UNDER TWO MAJOR HEADINGS

- (1) SINGLE PROCESSOR MESI IMPLEMENTATION
- (2) MULTIPROCESSOR MESI IMPLEMENTATION

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## EXAMPLE OF STATE TRANSITIONS



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## SINGLE PROCESSOR MESI - INITIAL READ FROM SYSTEM MEMORY

1. BECAUSE L1 & L2 STATE BITS ARE SET TO I, INITIAL READS ARE FORCED TO READ MEMORY
2. WHEN DATA IS PLACED INTO L1 & L2, THE L2 CACHE LINE IS SET TO THE E STATE, THE L2 CACHE LOWERS THE *WB/WT#* LINE TO INDICATE THAT THE LINE SHOULD BE STORED IN THE L1 CACHE IN THE S STATE

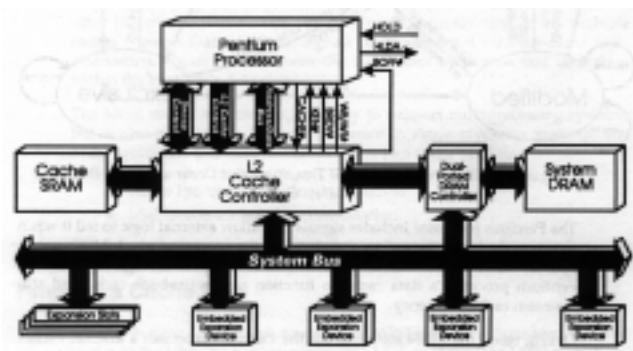
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## FIRST WRITE TO L1 CACHE LINE

1. THE L1 CACHE LINE IS UPDATED BY THE INTERNAL WRITE AND THE DATA IS WRITTEN THROUGH TO THE L2 CACHE
2. AFTER BEING UPDATED, THE L2 CACHE TRANSITIONS THE STATE BITS TO INDICATE THAT THE LINE HAS BEEN MODIFIED (M)
3. THE L2 CACHE RAISES THE *WB/WT#* LINE TO NOTIFY THE L1 CACHE TO TRANSITION THE LINE STATE FROM S TO E

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## CONTROL SIGNALS FOR LINE-FILLS



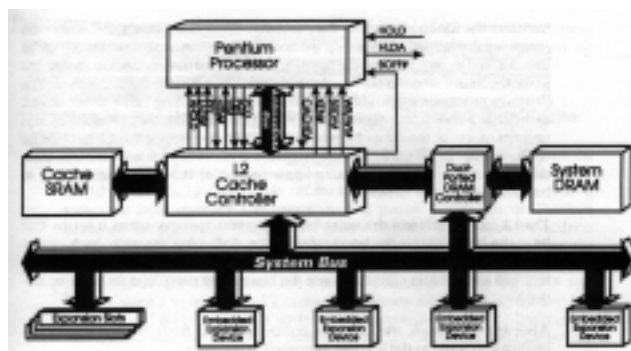
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## *BUS MASTER READ FROM LINE STORED IN M STATE IN L2 CACHE*

1. THE L2 CACHE SNOOPS THE ADDRESS.
2. IT BACKS OFF THE BUS MASTER.
3. THE L2 CACHE TRANSFERS THE ADDRESS TO L1 AND ASKS L1 CACHE TO SNOOP THE ADDRESS (USING *AHOLD*, *EADS#*, ...).
4. THE L1 CACHE TRANSITIONS THE LINE STATE BITS FROM E TO S.
5. THE L2 CACHE PERFORMS A WRITE-BACK TO MEMORY.
6. THE BACKOFF IS RELEASED TO ALLOW THE BUS MASTER TO READ THE TARGET LINE FROM MEMORY.
7. THE L2 CACHE TRANSITIONS ITS STATE FROM M TO S.

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## *SIGNALS FOR DEFINING STATES AFTER A SNOOP HIT*



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## ***BUS MASTER WRITE TO LINE STORED IN M STATE IN L2 CACHE***

1. THE L2 CACHE SNOOPS THE ADDRESS.
2. IT BACKS OFF THE BUS MASTER.
3. THE L2 CACHE TRANSFERS THE ADDRESS TO L1 AND ASKS L1 CACHE TO SNOOP THE ADDRESS. (USING *AHOLD*, *EADS#*, ...)
4. THE L1 CACHE TRANSITIONS THE LINE STATE BITS FROM E TO I.
5. THE L2 CACHE PERFORMS A WRITE-BACK TO MEMORY.
6. THE L2 CACHE TRANSITIONS ITS STATE FROM M TO I.
7. THE BACKOFF IS RELEASED TO ALLOW THE BUS MASTER TO WRITE THE TARGET LINE TO MEMORY.

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## ***SECOND AND SUBSEQUENT WRITES TO INTERNAL CACHE***

A SECOND WRITE TO AN INTERNAL CACHE LINE RESULTS IN THE LINE BEING MODIFIED IN THE L1 CACHE AND NO-WRITE THROUGH OCCURS TO THE L2 CACHE

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